REMARKS/ARGUMENTS

Upon entry of this amendment, claims 20-25 remain pending. Claims 20-25 were rejected under 35 U.S.C. §103(a) as being unpatentable over May, U.S. Patent No. 5,815,168. Reconsideration in view of the following remarks is respectfully requested.

The attached listing of claims presents previously presented claims for the Examiner's convenience.

The Cited Art

To clarify any misunderstanding as to May, Applicant submits the following elaboration on remarks previously filed (see Response mailed October 7, 2002). May is directed to a tile-based memory organization in which the tile size and shape are modifiable parameters (col. 6, lines 19-21). According to May, a "tile" is a rectangular area of a display image (col. 2, line 64-col. 3, line 4; see also Fig. 3A). In the type of tile-based organization disclosed by May, the pixels within a tile are stored at consecutive addresses in a memory, with pixels in the next tile starting at the next consecutive address (col. 3, lines 15-23; see also Fig. 3B). Data storage for one possible tiling is shown in Fig. 3B; the tiles in this case are 128 pixels wide and 16 lines tall, with a depth of one byte per pixel (col. 3, lines 1-4). The first 2048 bytes in the address space (which coincide with the first row of the memory device) store the pixels in the first tile in scan line format (i.e., starting with the pixels in scan line 1 and ending with pixels in scan line 16). The next 2048 bytes (the second row of the memory device) store the pixels in the second tile. May teaches that the tile size is preferably limited to the row width of the memory device (see col. 6, lines 39-43).

Regardless of the particular tile dimensions, May teaches that the pixels in a tile are stored at locations having sequential addresses, with the next tile starting at the next sequential address. This is shown explicitly by the formula May teaches for computing the address of a pixel from its screen position X, Y (col. 7, line 46-col. 8, line 2).

It appears that May never mentions that a memory device might have multiple arrays, let alone any data organization for such a device.

Claims 20-24 distinguished

Applicant previously argued that claim 20 would not have been obvious over May at least because May fails to disclose or suggest the step of "storing data representing each of said plurality of pixel groups, respectively, in a row of a plurality of non-adjoining arrays in the memory circuit." In response, the latest rejection of claim 20 asserted that it would have been obvious to modify May "by storing data in either an odd or even array when a received signal (video mode) comprises odd and even lines." Assuming arguendo that this is true, Applicant fails to see its relevance to claim 20. Claim 20 refers to pixel groups formed by segmenting "a plurality of pixels representing *one line* of an image display panel" (emphasis added) and does not recite any features related to odd versus even lines.

Applicant maintains that it has not been shown that May discloses or suggests the recited "storing" step. While dividing a display image into tiles, which May does teach, might relate to the recited step of "segmenting a plurality of pixels representing one horizontal line of an image ... into a plurality of pixel groups" (with each pixel group belonging to a different tile), May does not disclose or suggest that data for each pixel group could be stored in "a row of a plurality of non-adjoining arrays in the memory circuit." In accordance with May, pixels of the first tile (including a first pixel group) would be stored using addresses of a first row of a memory array. The second tile (including a second pixel group) would be stored starting at the next consecutive address after the last pixel of the first tile; assuming the first tile consumes a row, the second tile would start at the next row of the same array, as in Fig. 3B. Thus, rather than storing the data for each pixel group in "a row of a plurality of non-adjoining arrays" as recited in claim 20, May teaches storing the data for each pixel group in the *same* array.

Nothing in May suggests any other possibility. It is generally known in the art that in conventional memory devices that use multiple arrays, addresses are assigned consecutively across the first row of one array, then across the next row of that array, and so on until the end of the array. At that point the next consecutive address would be assigned to the first row of the next (adjacent) array. Since May only discloses storing data for adjacent tiles at

consecutive addresses, a person of ordinary skill in the art could infer, at most, that in the case where data for one tile is stored in the last row of an array, data for the next tile would be stored in an adjacent array. Thus, May does not teach or suggest at least the step of storing pixel groups of one line of an image display "in a row of a plurality of non-adjoining arrays in the memory circuit" as recited in claim 20.

For at least these reasons, claim 20 is patentable over May, and dependent claims 21-24 derive patentability from parent claim 20. Withdrawal of the rejection of claims 20-24 is respectfully requested.

Claim 25 distinguished

Applicant previously argued that May fails to disclose or suggest at least the steps of "storing pixel data from the first half of the panel in odd numbered arrays in the memory circuit"; and "storing pixel data from the second half of the panel in even numbered arrays in the memory circuit" as recited in claim 25. In response, the current rejection of claim 25 asserted that it would have been obvious to modify May "by dividing the display into respective portions based on the users needs and the type of signal to be displayed." This does not address Applicant's arguments.

Accordingly, Applicant again submits that the "storing" steps of claim 25 are not taught or suggested by May. As discussed above, May teaches that addresses are consumed sequentially for the pixels in each tile. May also teaches that tiles are arranged in rows across the display area (Fig. 3A). Thus, pixels for the upper half of the display area would all be stored with a first set of sequential addresses and pixels for the lower half of the display area would all be stored with a second set of sequential addresses. May is silent on ordering of addresses in multiple-array devices. As discussed above, a person of ordinary skill in the art would infer, at most, that each set of sequential addresses would correspond to adjacent arrays, not to "odd-numbered" and "even-numbered" arrays as recited in claim 25. There is no suggestion in May to deviate from the assignment of sequential addresses.

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For at least these reasons, claim 25 is patentable over May. Withdrawal of the rejection of claim 25 is respectfully requested.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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